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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wayne F. Ellis et al.

Serial No.: 10/707,797

Filed: January 13, 2004

Title: Integrated Redundancy Architecture And Method for Providing Redundancy Allocation to an Embedded Memory System

Attorney Docket No.: BUR920030151US1
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Group Art Unit: 2117

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Examiner: Guerrier Merant

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 4, 2009

RESPONSE TO FINAL OFFICE ACTION UNDER 37 C.F.R. § 1.116

This is in response to the Office Action mailed from the United States Patent and Trademark Office on November 7, 2008, with respect to the above-identified application.

A **Status of the Claims** starts on the following page 2.

Remarks concerning the Office Action start on the following page 6.